REMARKS

Claims 17-29 are pending in the above-referenced patent application.

Applicant amended independent claim 17 to clarify that the shifted value of the operand is loaded into one or more specified bytes of the local destination register indicated by the instruction. Support for this amendment may be found, for example, at page 11, lines 17-27 of the originally filed application. Applicant similarly amended independent claim 26. Applicant also amended claim 26 to correct the previous inadvertent omission of the word "more" preceding the wording "of a source register". Applicant also amended claims 22 and 27 to clarify that the field representing a mask specifies which byte or bytes of the destination register are affected.

The examiner rejected claims 17-29 under 35 U.S.C. §103(a) over the reference Computer Systems Design and Architecture by V. P. Heuring and H. F. Jordan (hereinafter Heuring), in view of the reference "Programming, Compiling and Executing Partially-Ordered Instruction Streams on Scalable Shared-Memory Multiprocessors" by D. K. Probst (hereinafter Probst).

Applicant's independent claim 17 discloses a local register instruction that loads one or more specified bytes within a local register with a shifted value of another operand. Applicant's instruction thus enables one or more of a register's bytes to be modified with a value from another source without affecting the value of the register's other bytes.

Heuring describes a RISC computer architecture and corresponding instruction set. For example, Heuring describes at pages 150 and 159-161, a shift instruction *shr*. As shown in the SRC Instruction Set summary (no page number available), the instruction *shr ra, rb, c3*, causes the processor to "shift rb right into ra by constant shift count c3 ≤ 31". As more particularly explained in Heuring's Table 4.5 and Table 4.10, on pages 150 and 160, respectively, the last step T7 in the execution of *shr* instruction causes the value of the operand C, which holds the shifted value held in *rb*, to be loaded into the destination register *ra* in its entirety. Thus, none of the various embodiments of the instruction *shr* as described by Heuring causes the value of an operand to be loaded into one or more specified bytes of a destination register, as required by

applicant's independent claim 17. Further, none of the RISC processor's other instructions, as listed in the SRC Instruction Set, causes a value of an operand to be loaded into one or more specified bytes of a destination register.

Probst discusses the performance of a large-scale shared-memory multi-processor architecture. Probst neither discusses the execution or the nature of specific instructions forming the multi-processors' instruction set, nor does it disclose an instruction that loads one or more specified bytes within a local register with a shifted value of another operand, as required by applicant's independent claim 17.

Thus, since neither Heuring nor Probst discloses or suggests, alone or in combination, applicant's claimed feature of "a local register instruction that loads one or more specified bytes within a local register with a shifted value of another operand", applicant's claim 17 is patentable over the applied references.

Claims 18-25 depend from independent claim 17 and are therefore patentable for at least the same reasons as claim 17. Independent claim 26 describes an apparatus featuring "a command that causes the ALU to load one or more specified bytes within a destination register of a selected microengine with a shifted value of another one or more bytes of a source register". For similar reasons as those provided with respect to independent claim 17, at least this feature is not disclosed by the art. Claim 27-29, which depends from claim 26, are patentable for at least the same reasons as claim 26.

Additionally, the examiner admits, with respect to claim 22, that "Heuring in view of Probst have not taught, a.Wherein the local register instruction comprises a field representing a mask that specifies which byte or bytes are affected" (paragraph 15, page 6 of the July 8, 2005, Office Action). The examiner, however, argues that the reference "Intel IA-64 Application Developer's Architecture Guide" (hereinafter Intel) teaches this feature.

Applicant's amended claim 22 discloses that the local register instruction of claim 17 comprises a field representing a mask that specifies which byte or bytes of the destination register are affected.

Intel describes mix instructions that enable interleaving of elements (e.g., bytes) from two source registers into a destination register (page 4-31, and pages 7-116-118). However, nowhere does Intel disclose that the mix instructions, or for that matter any other instruction, comprise a field representing a mask that specifies which byte or bytes of the destination register is affected by the instruction, as required by applicant's claim 22. Indeed, as illustrated in the various examples on page 7-117 relating to the operation of the mix instructions, all the bits of the destination register are populated with elements from the two source registers. Accordingly, since all the bits (and thus all the bytes) of the destination register are affected, there is no need for a mask that would specifies which particular bytes of the register that are to be affected by the instruction. So Intel does not disclose "wherein the local register instruction comprises a field representing a mask that specifies which byte or bytes of the destination register are affected".

Claims 23-24 depend from claim 22, and are thus patentable for at least the same reasons as claim 22.

Claim 27 recites the feature "wherein the command comprises a field representing a mask that specifies which byte or bytes of the destination register are affected". For similar reasons as those provided with respect to claim 22, at least this feature is not disclosed by the art. Claims 28-29 depend from claim 27 and are therefore patentable for at least the same reasons as claim 27.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim

does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply any charges or credits to deposit account 06-1050, referencing attorney docket No. 10559-320001.

Respectfully submitted,

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